



NEWS RELEASE

## Forte Announces Cynthesizer 3.4 with Automatic Power Management, Interface Generation, and ECO Flows

**San Jose, Calif. — May 21, 2008** — Forte Design Systems today announced the immediate availability of version 3.4 of its Cynthesizer™ SystemC synthesis product. Cynthesizer v3.4 adds features for significantly improving power results, automating design creation for synthesis from ANSI-C/C++ algorithms with high quality of results (QoR), and implementing engineering change orders (ECOs) for a seamless integration with ASIC and SoC flows.

### **Automatic Power Management with Power Compiler Integration**

Cynthesizer 3.4 adds integration for Synopsys' Power Compiler™, a key component of Synopsys' Galaxy™ Design Platform and Synopsys' comprehensive Eclipse™ Low Power Solution. At the RT level, Power Compiler enables fast and efficient trade-off analysis by performing automatic clock gating without requiring any changes to the RTL source. Power Compiler further reduces power during synthesis optimization by measuring trade-offs between positive timing slacks, area, and power and producing the lowest power-consuming design that meets user-defined timing and area constraints.

Power estimation reports generated by Power Compiler are included in the results available in the Cynthesizer Workbench, Cynthesizer's graphical interactive analysis environment. These reports, cross-linked to annotated source code views, make it easy to understand implementations tradeoffs and make changes for improved QoR. Users can find all of the analysis information they need easily in one place.

"Power is an important consideration for virtually every design today," said Brett Cline, Forte's vice president of marketing and sales. "Cynthesizer's silicon-proven quality of results for both datapath and control-based designs is now significantly enhanced with our integration with Power Compiler, as enabled through our membership in Synopsys' in-Sync Program. Our customers are now able to easily make tradeoffs between area, power, and performance."

### **Interface Generation Provides Higher Abstraction with Best QoR**

The new Cynthesizer Interface Generator creates highly customized, pre-verified interfaces for data communication between modules and threads in designs. This greatly improves the process of converting single-threaded C++ algorithms to multi-thread or multi-module hardware architectures raising the abstraction level available to designers.

The Interface Generator supports several types of custom interfaces, such as streaming, circular buffers, and shared memories. Each interface itself can be customized in terms of its specific data type, capacity, synchronization mechanism and other parameters. This technology makes it very

easy to build fully synthesizable data-transfer interfaces that are highly customized to designers' specific algorithms, resulting in efficient RTL quickly. It also makes it easy to substitute different interfaces for different configurations, thus allowing exploration of the optimum system architecture system without recoding.

### **ECO Capability with the New RTL Viewer**

Cynthesizer's new RTL Viewer allows provides designers with a graphical view for examining the RTL generated from the behavioral source including the various parts, functions, and registers and how they interact with each other. In addition, both SystemC and Verilog source can be viewed with annotations and links to the behavioral source as well as to other views available in the Cynthesizer Workbench. This tight link between the original algorithm and the resulting RTL provides an easy way to understand the relationship between the RTL and the behavior and to improve the quality of the RTL by applying various optimization techniques. ECOs can now be easily propagated from gates and RTL to the original SystemC source.

### **Pricing and Availability**

Forte's Cynthesizer v3.4 is available today from Forte. All the new features mentioned in this release are available at no additional charge to existing customers.

### **About Forte Cynthesizer**

Forte's advanced SystemC synthesis technology delivers production quality RTL in one tenth the time of hand coded RTL designs and eliminates downstream timing closure problems. Cynthesizer uses a high-level SystemC description to give designers the ability to build designs with custom interfaces and challenging architectural requirements not available with other C-based languages. Cynthesizer can automatically retarget designs to new speeds and process technologies without code changes and supports a level of reuse that is impossible in RTL. Cynthesizer is the practical, silicon-proven high-level synthesis solution you have been waiting for.

### **About Forte Design Systems**

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction. Forte's innovative high-level synthesis technology allows design teams creating complex electronic systems from algorithmic designs using ASICs, FPGAs, and SoCs to significantly reduce their overall design and verification time. Forte is headquartered at 100 Century Center Court, San Jose, CA 95112. For more information, visit <http://www.forteds.com/>.

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