



NEWS RELEASE

## Forte Adds Support for TLM Synthesis and Power Optimization Cynthesizer 3.0 Sets the Bar for ESL Synthesis

**San Jose, Calif. – January 23, 2006** - Forte Design Systems today announced the availability of the next generation of its Cynthesizer electronic system level (ESL) synthesis product. Cynthesizer v3.0 is the first ESL synthesis product to add support for SystemC transaction-level model (TLM) synthesis and automated Power Optimization.

"The transaction level is a substantially higher level of abstraction than standard behavioral level, and its advantages are compelling," said Brett Cline, vice president of Forte's customer operations and services group. "Version 3.0 of our industry-leading Cynthesizer not only further raises the abstraction level available to system and hardware designers by allowing them to create and implement arbitrarily high levels of abstraction, but our automated power optimization sets the bar for ESL synthesis capabilities."

### **TLM Synthesis Provides a Higher-level Abstraction**

Designers commonly run transaction-level models today for verification of complex ASIC and SoCs. The abstract communication mechanisms used in TLM, typically referred to as channels, pass information between design blocks by separating the interface from the algorithm and abstracting cumbersome hardware interface details from the designer while maintaining data coherency between the blocks. This standard modeling methodology raises the abstraction level, allowing the designer to model the design much more quickly and significantly increasing simulation performance about 25 times over pin-level behavioral and ~100x over RTL. It also establishes one verification environment for verifying the design at both the TLM level and RT level; any hardware block can be verified as soon as it is implemented.

Forte's TLM Synthesis represents the first behavioral synthesis offering to integrate high-speed SystemC TLM models with the implementation flow, maintaining a common source for simulation and implementation. Cynthesizer automatically creates high-quality RTL from the TLM representation by adding bus specific cycle-accurate pin-level hardware interface details. Because the process is automatic and fast, designers can easily change I/O interfaces to retarget their IP to a number of different interfaces and explore how various interfaces affect the overall quality of results, thus eliminating costly rewriting and risk.

To further help the designers achieve results quickly, Forte is providing synthesizable behavioral IP for fifos, memory interfaces, and streaming interfaces. Additionally, OSCI has recently added a set of classes in SystemC for TLM, in effect extending the vocabulary of design to include high-level communications. Forte's TLM synthesis directly supports the OSCI TLM library, and can be customized by Forte or by the user to support other TLM environments.

## **Power Optimization Capabilities Allow Early Design Tradeoffs**

Acceptable power characteristics are paramount to the success of many ASIC and SoC designs today, especially at 90 nanometers and below. Historically, optimization has typically been done in RTL at the end of the design cycle, where changes are often difficult and expensive.

Cynthesizer v3.0 adds support for power optimization early in design -- during the high-level synthesis process -- utilizing well-known techniques such as clock gating. Designers can now easily create multiple candidate RTL implementations which trade off area, performance, and power by directing Cynthesizer to meet certain design constraints in minutes rather than weeks or months. This gives designers the ability to pick the right implementation for their specific design constraints -- a capability not available using RTL.

## **Additional Features and QoR Optimizations**

Cynthesizer v3.0 adds support for Summit Design's Vista™ IDE for SystemC. Designers will be able to use Vista to quickly debug and verify behavioral design models and then pass models directly to Cynthesizer through its automation environment. Additionally, Cynthesizer v3.0 has a number of enhancements that further improve QoR of the RTL output and expand the synthesizable input available to the designers.

## **Pricing and Availability**

Cynthesizer v3.0 is available immediately starting at US\$250,000 for a 1-year time-based license. The TLM Synthesis and Power Optimization features are available as add-ons to Cynthesizer starting at US\$65,000 and US\$90,000, respectively.

## **About Forte Cynthesizer**

Forte's Cynthesizer significantly reduces the time needed to create complex chips and systems by automatically generating high-quality hardware designs from high-level algorithms. Cynthesizer is silicon-proven with uncompromising quality of results that often exceed hand-coded RTL. It is the only behavioral synthesis product that offers designers a complete environment including synthesis, verification, and co-simulation. Cynthesizer has been used on over 100 designs and is in production use in more than 15 of the top systems and semiconductor companies worldwide.

## **About Forte Design Systems**

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction. Forte's innovative high-level synthesis technology allows design teams creating complex electronic systems from algorithmic designs using ASICs, FPGAs, and SoCs to significantly reduce their overall design and verification time. Forte is headquartered at 100 Century Center Court, San Jose, CA 95112. For more information, visit [www.ForteDS.com](http://www.ForteDS.com).

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